

Hyoukjun Kwon

PH.D. STUDENT

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Research Interest

Interconnection network (NoCs)

Computer architecture

Reconfigurable architecture

Machine learning

Design automation

Hardware security

Education

Georgia Institute of Technology

Ph.D. student in Computer Science

Aug. 2015 - Current

Advisor: Dr. Tushar Krishna

SNU (Seoul National University)

B.S. in CSE (Computer Science and Engineering)

Mar. 2007 - Feb. 2015

B.S. in EMS (Environmental Material Science)

Advisor: Dr. Jihong Kim (CSE) and Dr. Junjae Lee (EMS)

Professional Experience

Georgia Institute of Technology, Atlanta, GA

Graduate Research Assistant

Aug. 2015 - present

NVIDIA Research, Westford, MA

Research Intern at architecture research group (ARG)

May 2017 - Aug. 2017

Talks

MAERI: Enabling Flexible Dataflow Mapping over DNN Accelerators via Reconfigurable Interconnects

ASPLOS 2018, Williamsburg, Virginia

Mar. 2017 (to be presented in the conference)

OpenSMART: An Opensource Single-cycle Multi-hop NoC Generator

SC17 OpenSuCo 2017, Denver, Colorado

Nov. 2017

Rethinking NoCs for Spatial Neural Network Accelerators

NOCS 2017, Seoul, Korea

Oct. 2017

Adaptive Manycore Architectures for Big Data Computing

NOCS 2017, Seoul, Korea

Oct. 2017

Light-weight and High-performance NoC for DNN accelerators

Konkuk University, Seoul, Korea

Oct. 2017

Proving Flow Security of Sequential Logic via Automatically-Synthesized Relational Invariants

CSF 2017, Santa Barbara, California

Aug. 2017

Optimizing Networks-On-Chip for Deep Learning Accelerators using Micro-Switches

NVIDIA Research, Westford, Massachusetts

Aug. 2017

Automatic generation of low-latency networks-on-chip

Bluespec Inc., Framingham, Massachusetts

Jul. 2017

OpenSMART: Single-cycle Multi-hop NoC Generator in BSV and Chisel

ISPASS 2017, Santa Rosa, California

May. 2017

Publications

Hyoukjun Kwon, Ananda Samajdar, and Tushar Krishna, “*MAERI: Enabling Flexible Dataflow Mapping over DNN Accelerators via Reconfigurable Interconnects*”, *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2018 (will appear in the conference)

Brian Lebednik, Sergi Abadal, **Hyoukjun Kwon**, and Tushar Krishna, “*Spoofing Prevention via RF Power Profiling in Wireless Network-on-Chip*”, *International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems (AISTECS)*, 2018

Hyoukjun Kwon, Ananda Samajdar, and Tushar Krishna, “*Rethinking NoCs for Spatial Neural Network Accelerators*”, *International Symposium on Networks-on-Chip (NOCS)*, 2017

Janardhan Rao Doppa, Ryan Gary Kim, Mihailo Isakov, Michel A. Kinsy, **Hyoukjun Kwon**, and Tushar Krishna, “*Adaptive Manycore Architectures for Big Data Computing*”, *International Symposium on Networks-on-Chip (NOCS)*, special session paper, 2017

Hyoukjun Kwon, William Harris, and Hadi Esmaeilzadeh, “*Proving Flow Security of Sequential Logic via Automatically Synthesized Relational Invariants*”, *Computer Security Foundations (CSF)*, 2017

Hyoukjun Kwon and Tushar Krishna, “*OpenSMART: Single-Cycle Multi-hop NoC Generator in BSV and Chisel*”, *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2017

Hyoukjun Kwon, Dohyun Kim, Jisung Park, and Jihong Kim, “*Improving the Lifetime of NAND Flash-based Storages Using MADE (Minhash-Assisted Delta-compression Engine)*”, *Korean Institute of Information Science and Engineers Annual Conference (KIISE)*, 2014

Research Projects

Enabling flexible dataflow in DNN accelerators

NVIDIA and Georgia Institute of Technology

May. 2017 - PRESENT

- Developed a light-weight and reconfigurable NoC architecture to support flexible dataflow in DNN accelerators
- Developed a dataflow evaluation framework that can be plugged into DNN accelerator RTL

DARPA - CHIPS project (Communication architecture support for highly modular chip design)

Georgia Institute of Technology

Sep. 2017 - PRESENT

- Developing communication protocol and hardware for highly modular chip design.
- Will provide a generator that can be integrated in CAD tools

A communication-aware flexible dataflow DNN accelerator (MAERI)

Georgia Institute of Technology

Jan. 2017 - Jan. 2018

- Developed a new DNN accelerator microarchitecture for CNN and RNN that offloads computation into network side and maximize the utilization of computation units.
- Implemented RTL using Bluespec System Verilog.
- Implemented a design space exploration tool that optimizes the accelerator architecture under user-defined optimization goal and constraints.
- Published a paper as the first author in ASPLOS 2018.

Secure wireless NoC system

Georgia Institute of Technology

Aug. 2016 - Jan. 2018

- Worked on a method that prevents hardware Trojan that monopolies wireless network channel bandwidth and slows down other cores.
- Published a paper as a co-author in AISTECS 2018

Scalable NoC design for DNN accelerators

Georgia Institute of Technology

Aug. 2016 - May. 2017

- Developed a light-weight and low-latency interconnection network for CNN accelerators.
- Implemented distributed architecture of network fabric that maximizes PE utilization.
- Implemented RTL using Bluespec System Verilog.
- Published a paper as the first author in NOCS 2017.

Advanced low-latency network-on-chip generator

Georgia Institute of Technology

Nov. 2015 - Oct. 2016

- Developed a network-on-chip RTL generator that provides state-of-the-art mesh and single-cycle-multi-hop (SMART) network.
- Verified the design comparing RTL simulation results with those of Garnet under synthetic workloads and synthesized the design for ASIC and FPGA
- Provided the source code as opensource; now it is used by Bluespec Inc. IIT Madras for RISC-V Shakti Project, and Intrinsix Corp. for the DARPA CHIPS project
- Published a paper as the first author in ISPASS 2017.

Information flow-secure FPGA accelerators

Georgia Institute of Technology

Oct. 2015 - Aug. 2016

- Developed an information flow policy language and a policy checker using a state-of-the-art formal verification method.
- Successfully identified insecure open-source hardware designs within several minutes on a laptop.
- Published a paper as the first author in CSF 2017.

Endurance-aware flash transition layer design

Seoul National University

Dec. 2014 - Sept. 2015

- Developed an FTL (flash-transition-layer) that delta-compresses write data toward flash memory and efficiently manages the mapping information of delta-compression
- Reduced significant write traffic toward flash memory, which enhances the lifetime of flash memories.
- Published a paper as the first author in KIISE 2014.

Teaching

Special Lecture: Designing a CNN Accelerator Using Bluespec System Verilog

Seoul National University

Dec. 2017

- Taught a 3-day course about CNN accelerator design for CS and ECE undergraduate students.
- Developed lecture materials and lab code, which lets students implement a full CNN accelerator.

Teaching assistant in processor design course

Georgia Institute of Technology

Jan. 2017 - May 2017

- Helped students with processor design assignments on Altera FPGA boards.
- Graded exams and assignments

Teaching assistant in computer architecture course

Seoul National University

Sep. 2014 - Dec. 2014,
Mar. 2015 - Jun. 2015

- Developed lab assignments that implements a Y86 processor in Bluespec System Verilog.
- Verified the Y86 processor design on an FPGA.
- Helped developing course material.

Skills

Software languages

C/C++, JAVA, VBA, OCaml, Scheme, Matlab, and LaTeX

Formal verification tools

Coq Proof Assistant and ABC

Hardware languages

Verilog, Chisel, System C, and Bluespec System Verilog

ASIC synthesis tools

Synopsys Design Compiler and Cadence Encounter(Innovus)

FPGA synthesis tools

Xilinx Vivado and Altera Quartus

Parallel programming

OpenMP, OpenCL, and MPI

Image processing

Matlab

Languages

Korean, English, and Japanese